$(Pb,Sr)TiO_3$ Thin Films for a ULSI DRAM Capacitor Prepared by Liquid Source Misted Chemical Deposition

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To overcome the limitations of conventional capacitor structure, ferroelectric thin films, for example, Pb(Zr, Ti)O_3 (PZT),[1] $SrBi_2Ta_2O_9$ (SBT),[2] and (Ba,Sr)TiO_3 (BST),[3] have been intensively studied for a number of integrated devices such as dynamic random access memories (DRAM) and nonvolatile random access memories (NVRAM) because of high dielectric constant, large spontaneous polarization, and low leakage current. Among the various ferroelectric films, BST thin film was noticed as the most promising material for the capacitor of a ULSI DRAM cell due to its high dielectric constant and paraelectricity at normal operating temperature. Although BST possesses a satisfactorily high dielectric constant, BST capacitors have a rather low onset field for high current emission, that is, only 300−500 kV/cm, which will limit its minimum thickness that can be applied. Also, it was known that a post-heat-treatment at high temperature, 700 °C, was essential for obtaining good electrical property. Heat treatment at high temperature can have a poor effect on electrodes, barrier metals, and contact plugs.[4]

Strontium titanate ($SrTiO_3$) is one of the few titanates that is cubic at room temperature, but the dielectric constant is lower than BST. The addition of lead into strontium titanate makes its dielectric constant higher and the temperature of crystallization lower than BST. Also, the curie point, that is, the transition temperature from the ferroelectric (tetragonal) to paraelectric (cubic) phase, is retained to somewhere around or below room temperature, making (Pb,Sr)TiO_3 (PST) a paraelectric material with a high dielectric constant. Therefore, a PST thin film can be a promising material for the capacitor of a ULSI DRAM cell due to its high dielectric constant and paraelectricity at normal operating temperature.

Table 1. Growth Conditions for Preparation of a PST Thin Film by LSMCD

liquid source temperature	R.T. ∼ 50 °C
pressure during deposition	500−760 Torr
frequency of sonicator	1.63 MHz
baking	400−500 °C for 5 min
annealing	550−700 °C for 30 s to ≈30 min
typical deposition rate	5−20 nm/min
Ar flow rate	200−2000 sccm
wafer	Si(100), Si(100)/SiO_2(500 nm)/Pt(100 nm)
top electrode	Pt(100 nm) by sputtering
rotating speed	0−300 rpm

According to the progress of thin film technology, a number of studies on ferroelectric thin films are available in the literature. The deposition methods of BST thin films by several techniques such as dry methods (sputtering,[5] laser ablation,[6] and chemical vapor deposition (CVD)[7]) and wet methods (sol−gel,[8] metalorganic decomposition (MOD),[9] and liquid source misted chemical deposition (LSMCD))[10−15] have been studied. Among these, in general LSMCD has the advantages of good reproducibility of composition, high deposition rate, and the easy selection of metal precursors without the limitation of high vapor pressure at low temperature in CVD. In particular, the reproducibility of composition is one of the important parameters for obtaining the desired electrical properties.

In this study, PST thin films were prepared by the LSMCD method using Pb acetate [$Pb(OOCCH_3)_2$], Sr acetate [$Sr(OOCCH_3)_2$], and Ti isoproxide [$Ti(O^iC_3H_7)_4$] as metallic precursors. These were dissolved in acetic acid and 1-butanol. An ultrasonic nebulizer (HU-350, Samsung Electronic Co., Ltd. frequency of sonicator: 1.63 MHz) was used to make the mists of the precursor solution. The mist was transported to a deposition chamber by a carrier gas (Ar). The Si(100) and Pt-coated Si (Si(100)/SiO_2(500 nm)/Pt(100 nm)) were used as wafers. The deposited PST thin film was baked at 400 °C for 10 min. The films were subsequently annealed in the range of 500−700 °C for 5 min in rapid thermal annealing (RTA). The thickness of a film was controlled by repeated deposition. The detailed growth conditions of PST thin films are shown in Table 1. The structure and surface morphology of PST thin films were characterized by X-ray diffraction (XRD) and scanning electron microscopy (SEM). The composition of the thin film was analyzed by using wavelength dispersive spectroscopy (WDS). Also, the depth profile was ob-

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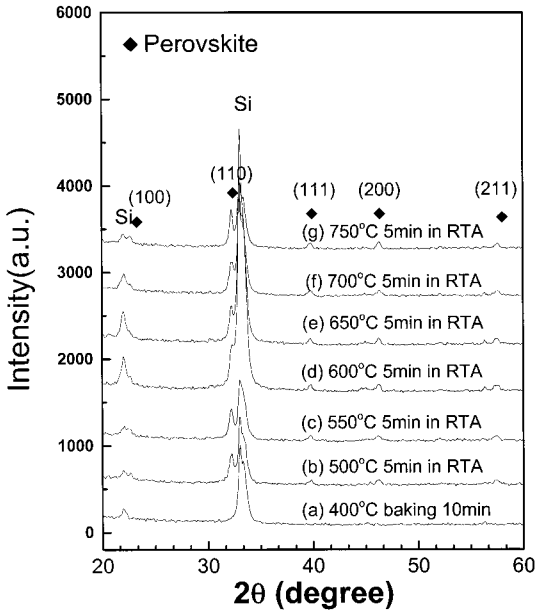

Figure 1. XRD patterns of PST thin films on a Si(100) wafer annealed at various temperatures.

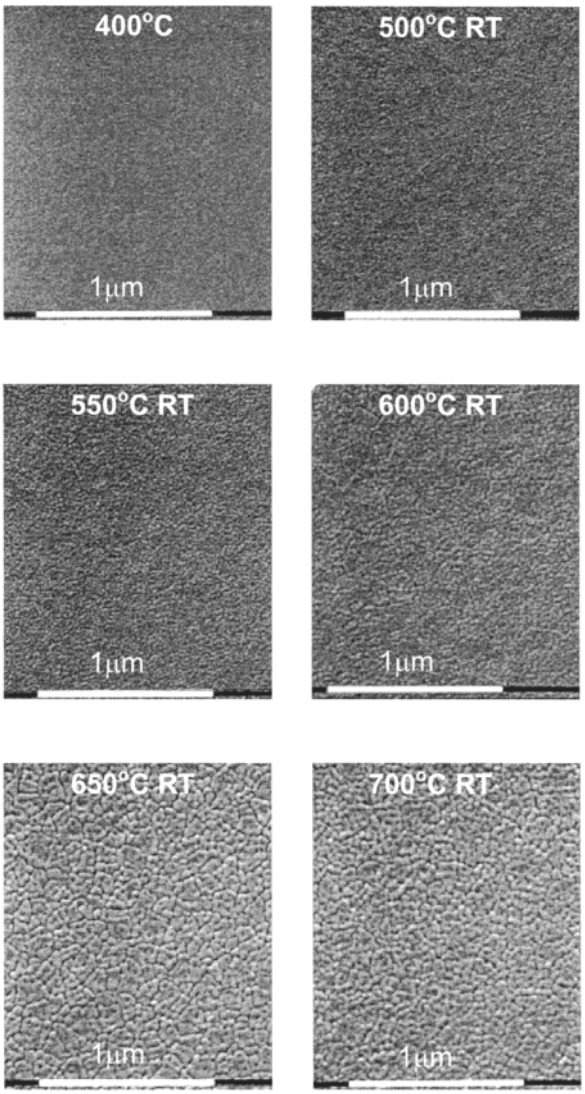

Figure 2. SEM photographs of PST thin films on Pt-coated Si(100) wafers annealed at various temperatures.

tained by using auger electron spectroscopy (AES). To measure electrical properties, we prepared a Pt upper

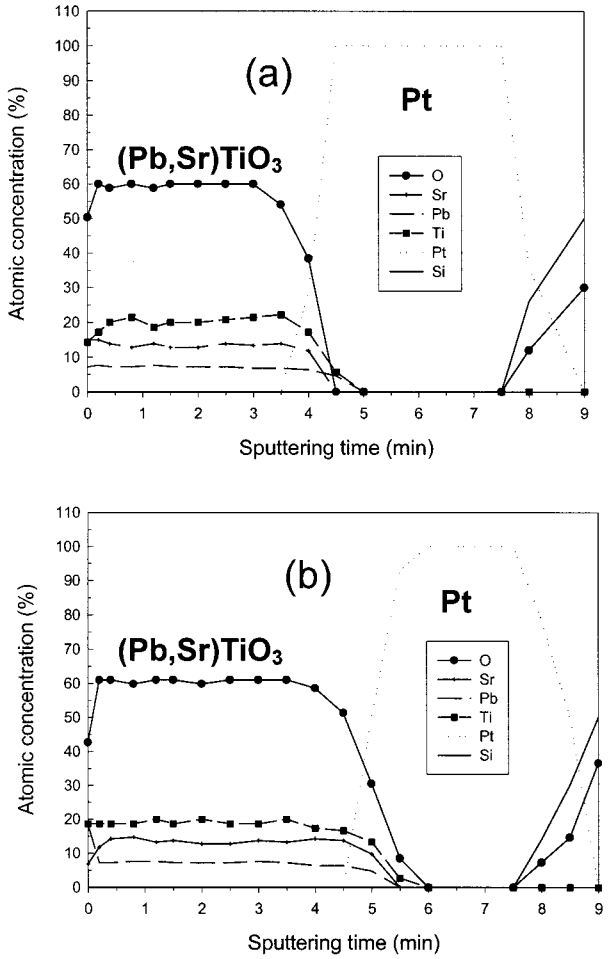

Figure 3. AES depth profiles of PST thin films annealed at (a) 550 °C and (b) 650 °C for 5 min in RTA.

electrode of 400 μm diameter by using a shadow mask in the rf-magnetron sputter. Capacitance-voltage (C−V) and leakage current (I−V) characteristics were measured by using an impedance analyzer (HP4192A) at 100-kHz frequency and picoampere current meter (HP4145B) with the conditions of 0.05 V of step voltage and 1 s of delay time, respectively.

As-deposited PST films (150-nm thick) were baked in air at 400 °C and annealed in air at the various temperatures for 5 min by RTA. Their crystal structures on Si(100) were examined by XRD with Cu Kα radiation as shown in Figure 1. The crystallization occurred at 500 °C. A polycrystalline phase such as (100), (110), (111), and (211) was formed. The surface morphologies of PST thin films are shown in Figure 2. The grains were observed above 500 °C. This result is consistent with that of XRD. It can be seen that the surface of the PST film is very smooth, dense, and uniform without cracks and void. The mean grain size of the film annealed at 650 °C was about 23 nm calculated by Scherrer's formula.[16]

The elemental component distribution of PST thin film on the Pt-coated Si substrate and the contaminants on the surface of PST thin film were obtained by using auger electron spectroscopy (AES) as shown in Figure 3. Figure 3a is the AES depth profile of PST thin film (100-nm thick) annealed at 550 °C for 5 min. The component concentration is nearly uniform through the whole bulk of PST film. Carbon signals were observed

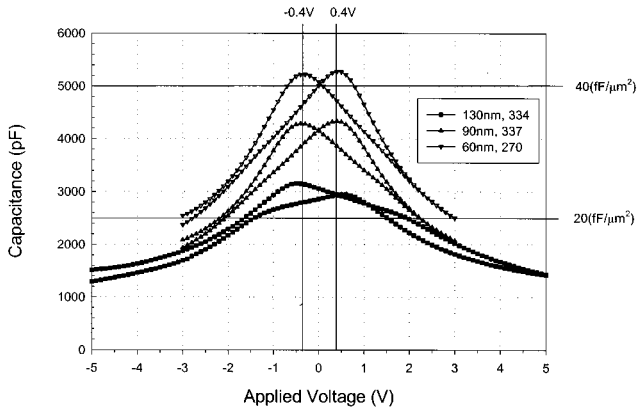

Figure 4. Capacitance−voltage curves (at 100 kHz) of the PST thin films annealed at 550 °C for 5 min in RTA.

at the surface of PST thin film in the derivative peak-to-peak data of AES. Figure 3b is the AES depth profile of PST thin film (130-nm thick) annealed at 650 °C for 5 min. The intensity of the carbon signal was smaller than that of (a) at the surface of the PST thin film. However, the components of Pb and O were abnormal at the surface of the PST thin film. This might have resulted from the high mobility and high evaporation of Pb above 640 °C. However, the component concentration was nearly uniform through the whole bulk of the PST film. The elemental composition of the deposited film at the various annealing temperatures was obtained by using WDS. The results revealed that the elemental composition of PST thin film is not different with that precursor solution. The change in the composition did not occur at a lower annealing temperature below 640 °C.

The capacitance−voltage curves (at 100 kHz) of the PST thin films annealed at 550 °C for 5 min in RTA are shown in Figure 4, where the data were taken using an HP4192A impedance analyzer. The atomic ratios of Pb/(Pb + Sr) and Ti/(Pb + Sr) are 0.36 and 1.06, respectively. A slight ferroelectric property is indicated by the butterfly-type capacitance−voltage curve. But the voltage of the highest capacitance is smaller than that of a typical ferroelectric thin film such as PZT. So the paraelectricity of the PST thin film might be obtained by a decrease of Pb content. The dielectric constant and dielectric loss obtained here are almost the same at 330

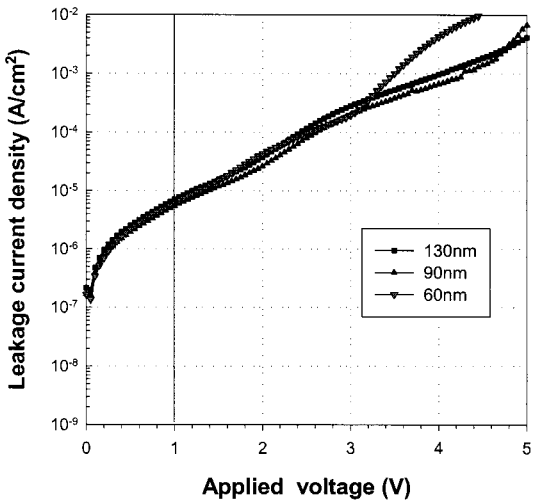

Figure 5. Current−voltage characteristics of the PST thin film annealed at 550 °C for 5 min in RTA.

and 0.04 from 130- to 90-nm thick at 0 V, respectively. The dielectric constant decreased below 60-nm thick. But its equivalent oxide thickness was similar, about 0.9 nm. The current−voltage characteristics of the PST thin films annealed at 550 °C for 5 min in RTA are shown in Figure 5. The current−voltage curve on a PST thin film was measured by using an HP4145B picoampere current meter. The atomic ratios of Pb/(Pb + Sr) and Ti/(Pb + Sr) are 0.36 and 1.06, respectively. The leakage current density of PST thin film (90-nm thick) is less than 5.5×10^{-6} A/cm^2 at an applied voltage of 1 V. The lower leakage current density might be obtained by using postannealing under O_2.

Polycrystal PST thin films have been successfully grown on Pt-coated Si(100) wafers by the LSMCD method. XRD, SEM, AES, and WDS studies show the PST thin film has high crystallinity, a smooth surface, and uniform elemental composition at a low annealing temperature, respectively. Electrical measurements reveal a PST thin film has a high dielectric constant, low dielectric loss, and good insulating properties. These results indicate that a PST thin film is a promising material for a ULSI DRAM capacitor and other microelectronic device applications.

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